

CGRS Microtech Inc.

## DATA 1

Data Acquisition And Control System

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#### 1) INTRODUCTION

The CGRS Microtech DATA 1 is a printed circuit board which adds data acquisition and control capability to the Commodore 64.

It contains five sections:

- 1) Analog to Digital Converter
- 2) Digital to Analog Converter
- 3) Digital Inputs
- 4) Digital Outputs
- 5) Real Time Clock

## 2) General Description

The DATA 1 is supplied with a 5.25 inch diskette which contains software that controls all on-board devices, and allows easy data transfer between all devices. To load all the software, perform the following two loads:

LOAD "MACODE",8,1

LOAD "BRTC",8

The Data 1 board plugs into the expansion connector of the commodore 64. The +5V DC supply voltage is provided from the 64. The on board +12V DC, -12V DC are generated using DC-DC converters. These voltages provide power for the A/D converter and the D/A converter. The ribbon cable headers are provided for connection to external devices. All devices on board are memory mapped into the area from \$DFFC to \$DFFF. They may be accessed from basic, forth, machine code etc. Drivers are provided on diskette which allow the user to communicate with each device easily. See each section for detailed operating instructions.

The DATA 1 board uses an Intersil ICL7109 12 bit A/D converter chip. This chip allows analog voltages to be converted into digital form and placed into the Commodore's memory. A 16 channel analog multiplexer ( IH6116 ) steered by the channel register together with the ICL7109 provides 16 seperate analog inputs. The input voltage range is from 0 to 10 volts. (This is adjustable by changing the precision resistors between the mux and the A/D.) The internal reference of the 7109 provides the precision refernce voltage required by the A/D converter. A voltage divider R7 and R8 divide the 0-10 volt signal down to a 4.096 full scale voltage which the ICL7109 accepts as its input range. The range can be modified by changing the precision resistors R7 and R8. The conversion value may be scaled by adjusting potentiometer R10 which changes the reference voltage. The Reference voltage is factory set at 2.096 VDC. In order to obtain a channel measurement, the following procedure should be followed:

- 1) Load the Basic file "BRTC".
- 2) Place the desired A/D channel into the variable CHAN in line 1010.
- 3) Run the program starting at line 1000 and the 12 bit decimal value will be printed on the screen.

## 4) DIGITAL TO ANALOG CONVERTER

The DAATA 1 board uses an Analog Devices 7542N 12 bit D/A converter. The D/A provides an analog voltage directly proportional to the contents of its 12 bit register. An on board pin programmable precision voltage reference AD584 provides precision output voltages of 10.000V,7.500, 5.000V and 2.500V. This voltage is fed to the DAC to form the full scale voltage output. The output voltage is programmable from on board jumpers. The 12 bit value to be written to the DAC is first placed in two bytes of Ram. A machine language routine is then called to transfer the two bytes of information from Ram to the DAC 12 bit output register. An AD542 precision BiFet op amp is used as the Dac output amplifier.

To place a 12 bit value into the DAC registers:

- 1) Load the file "BRTC" from the supplied diskette. Load the Machine Code file "MAC-CODE", 8,1 from the diskette.
- 2) Set the variable LOBYT in line 2040 to the desired 8bit lo byte value and the variable HIBYT in line 2050 to the desired high 4 bit nibble. Always set the 4 most significant bits of HIBYT to zeroes.
- 3) Type RUN 2030 and the DAC output will reflect the value placed in it's registers. To clear the DAC registers type run2020.

## 5) DIGITAL OUTPUTS

The DATA 1 uses a 74LS374 octal latch and a 74LS174 hex latch to provide 10 TTL compatible digital outputs. The outputs may be used to drive digital displays, control multiplexers, solid state relays etc... The value to be written to the outputs is poked from BASIC to transfer data to the output registers.

To place bits 0-7 on the first port:

POKE 57343, VALUE1

Each bit of VALUE1 represents a power of 2 from 2\*\*0 to 2\*\*7.

bit1=2\*\*0=1

bit2=2\*\*1=2 etc.

All bits are summed together to form the decimal value to be poked to location 57343.

To place bits 8,9 on the second port: POKE 57342, VALUE2

The first four bits of VALUE2 are the A/D Converter channel address bits. The fifth and sixth bits of VALUE2 are the ninth and tenth digital outputs.

The outputs must be buffered to drive conventional type relays or devices requireing more current than 2.6mA at +5VDC. and 24mA at ground.

## 6) DIGITAL INPUTS

The DATA 1 uses a 74LS244 Octal buffer and a 74LS367 hex buffer to provide 12 TTL compatible (0-5V) digital inputs. The inputs allow monitoring of switches, contact closures an other TTL logic etc...They are read in the following manner.

To read Inputs 0-7 PRINT PEEK ( 57343 )

Once again each bit represents a power of 2 from 2\*\*0 to 2\*\*7.

To read inputs 8-11 PRINT PEEK ( 57342 )

The first two inputs of this latch are for monitoring the run status of the real time clock and the A/D Converter. Mask them off and look at the 4 most significant bits.

## 7) REAL TIME CLOCK

The DATA 1 board uses an OKI MSM58321RS Cmos real time clock calender chip. This crystal controlled chip allows the Commodore 64 computer to keep track of the year, month, day of month, day of week, hours, minutes and seconds.

A basic program (BRTC) prompts the user to enter the time and date and places this into Ram. They are later transferred into the 58321 registers using a machine language program (MC). When you wish to print the time and date on the screen, just call the 'Basic' subroutine and the information will appear on the screen. An on board battery keeps the Real Time Clock running when the power is not available. Set the clock once and forget it. The battery should be replaced once a year.

To load the real time clock softwaretype Load "brtc", 8 with the supplied diskette in the disc drive. When READY appears, type Load "MC", 8,1 to load the machine code program.

To enter the time and date type RUN 500, once the DATA 1 software has been loaded. The program will prompt you for the year, month, day of month, day of week, hours, minutes and seconds. Enter all parameters and the program will load them into the RTC chip and perform a read afterwards.

To read the time and date just type RUN. The time and date as well as a header will appear on the screen. Modifications may be made to the format of the print statements as necessary, or eliminated completely if events based on times are required to be initiated.

## DATAONE CONNECTOR PIN OUT

Connector J3 has all even number pins connected to ground. All odd number pins are signal level.

J3 is all analog input signals.

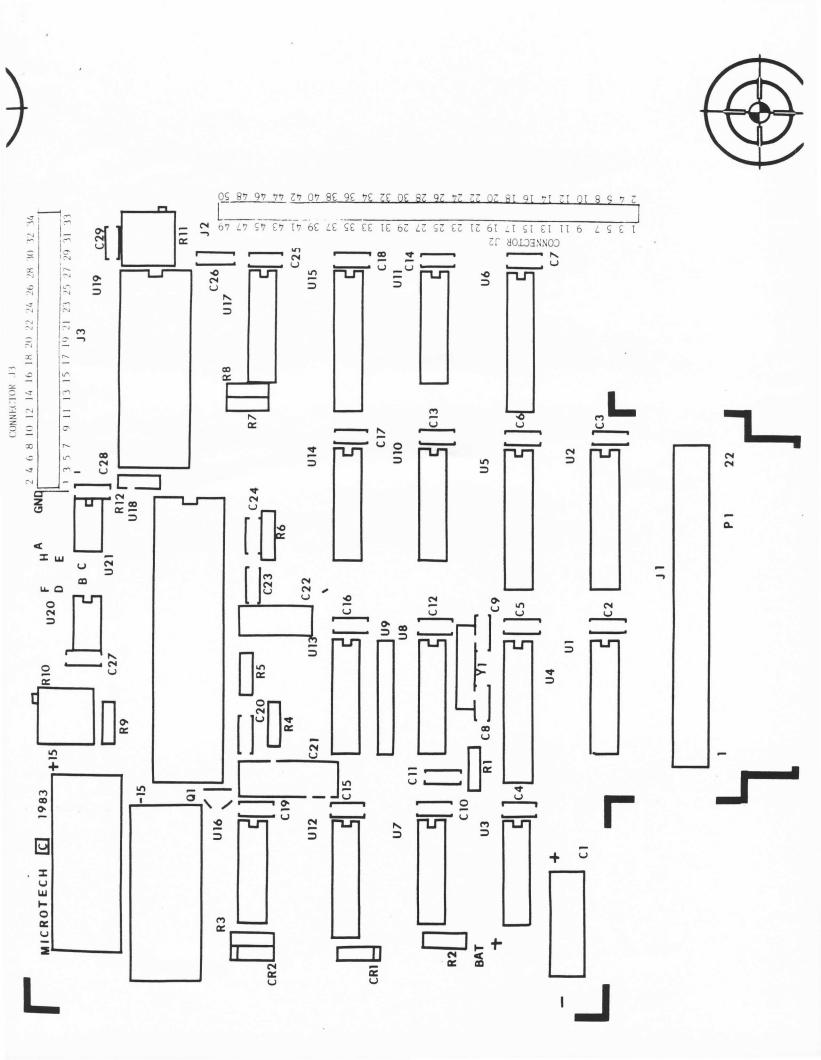
PIN	NUMBER	DESCRIPTION ANALOG INPUT
7		AIO
11		AI 1
15		AI 2
19		AI 3
23		AI 4
27		AI 5
31		AI 6
33		AI 7
3		AI 8
5		AI 9
9		AIIO
13		AI11
17		A I 1 2
21		AI13
25		A I 1 4
29		AI15

## ANALOG OUTPUT

The analog output signal is to the left of J3 and it is labled A and GND.

Connector J2 is used for all the digital input and digital output signals.

PIN NUMBER	DISCRIPTION
	DIGITAL INPUT
15	DI O
7	DI 1
13	DI 2
5	DI 3
11	DI 4
3	DI 5
9	DI 6
1	DI 7
23	DI 8
17	DI 9
19	DI10
21	DI11
	DIGITAL OUTPUT
39	DO O
3.7	DO 1
35	DO 2
33	DO 3
31	DO 4
29	DO 5
2 7	DO 6
25	DO 7
41	DO 8
43	DO 9



## END OF MAE PASS!

```
0040
                         .0S $9400
.DE $DFFF
              0050 INIT
              0060 STAT
                            . DE $DFFE
                            DE $DFFD
              0070 DDAD
              0080 CTBUF
0090 ARR
                            DE $DFFC
9400-
                            .DS 15
                                               ARRAY STORAGE
              0100
              0110 BUSY
940F- 48
                            FHA
              0120
                           LDA STAT ; LOAD STATUS OF RTC BUSY
9410- AD FE DF 0130 CHK
                           AND #01
9413- 29 01 0140
                                               ; MASK OFF ALL BUT RTC STA
9415- FO F9
             0150
                            BEQ CHK
                                               ; YES-CHECK AGAIN
9417- 68
              0150
                            FLA
                                               : NO-RETURN
                           RTS
9418- 60
              0170
              0180
              0190
                            ;
             0200 READ PHA
9419- 48
                                               : SAVE A
941A- 8A
941B- 48
             0210
                             TXA
             0.220
                            FHA
                                               ; SAVE X
9410- A9 00
             0230
                            LDA #00
                                               ; DISABLE ALL CTRL LINES,
941E- 8D FC DF 0240
                            STA CTBUF
9421- A2 OB 0250
9423- CA 0255 AGA
                            LDX #13
              0255 AGA
                           DEX
                                                FPLACE RTC ADDR ON BUS
9424- BE FD DF 0260
                            STX DDAD
9427- 20 OF 94 0270
                             USR BUSY
942A- A9 01 0280
942C- 8B FC BF 0290
942F- EA 0300
                            LDA #01
                                             ; RAISE ADDR WR LINE
                            STA CTBUF
942F- EA
                            NOP
9430- A9 10 0310
9432- 8D FC DF 0320
9435- A9 13 0330
9437- 8D FC DF 0340
943A- EA 0350
                            LDA #$10
                                                ; LOWER AD WR LINE, DISABL
                             STA CTBUF
                            LDA #$13
                                                / RAISE READ LINE
                            STA CTBUF
                            NOF
943B- EA
              0360
                            NOP
             0370
9430- EA
                            NOP
943D- EA
              0380
                             NOF
943E- EA
              0390
                             NOF
943F- EA
              0400
                             NOF
                                               ; READ RIC REG
9440- AD FC DF 0410
                            LDA CTBUF
9443- 29 OF
                             AND #15
             0420
                                          ; STORE IN ARRAY
9445- 9D 00 94 0430
                            STA ARR, X
9448- A9 OA
                            LDA #10
                                                ; LOWER READ LINE
              0440
                             STA CTBUE
944A- 8D FC DF 0450
                                                ; SET N FLAG
944D- 8A
             0460
                             TXA
944E- DO D3
             0470
                            BNE AGA
9450- 68
              0480
                             FLA
                                               ; RESTORE X
9451- AA
              0490
                             TAX
                                                ; RESTORE A
9452- 68
                            PLA
              0500
9453- 60
                            RTS
              0510
              0520
                            i
              0530
                             ;
              0540
```

9454- 48	0550 WRITE	PHA	j	SAVE A
9455- BA	0560	TXA		
9456- 48	0570	FHA	j	SAVE X
9457- A9 00	0580	LDA #00	j	DISABLE CTRL LINES
9459- 8D FC DF	0590	STA CTBUF		
945C- A2 OD	0600	LDX #13	;	# OF RTC REGIS
945E- CA	0405 DEC	DEX		
945F- 8E FD DF	0610	STX DDAD	,	PUT REG ON B BUS
9462- 20 OF 94	0620	USR BUSY		
9465- A9 01	0630	LDA #01		
9467- 8D FC DF	0640	STA CTBUF	;	RAISE AW, KEEP DDAD ENAB
946A- EA	0450	NOP		
946B- A9 00	0660	LDA #00	ì	LOWER AW TREEP DOAD ENAB
946D- 8D FC DF	0670	STA CTBUF		
9470- BD 00 94	0680	LDA ARR, X	;	FETCH DATA FROM ARRAY
9473- SD FD DF	0690	STA DDAD	;	PLACE DATA ON B BUS
9476- A9 02	0700	LDA #02	i	RAISE WR LINE
9478- 8D FC DF	0710	STA CIBUF		
947B- EA	0720	NOP		
947C- EA	0730	NOP:		
947D- EA	0740	NOP		
947E- A9 00	0750	LDA #OO	j	LOWER WR LINE
9480- 8D FC DF	0760	STA CTBUF		
9483- 8A	0770	TXA		
9484- DO D8	0780	BNE DEC		
9486- A9 10	0790	LDA ##10	j	DISABLE DDAD REG
9488- 8D FC OF	0800	STA CTBUF		
748B- 68	0810	PLA		
948C- AA	0820	TAX	į	RESTORE X
948D- 68	0830	FLA	;	RESTORE A
948E- 60	0840	RTS		
	0350	. EN		
END OF MAE PASS!				

--- LABEL FILE. ---

666 =9423 CHK =9410 DEC =945E STAT =DFFE 770000,948F,948F ARR =9400 CTBUF =DFFC INIT =DFFF WRITE =9454 808Y =940F 0DAB =0FFD READ =9419

## END OF MAE PASS!

```
; FILE "A7542"
                 0010
                                  : D/A MACHINE CODE DRIVER
                 0015
                                          AD7542UN
                                    DAC
                 0016
                 0020
                                  . BA $94A0
                 0030
                                  . OS $94AO
                 0040
                 0050 CIBUF
                                   DE $DFFC
                 0040 DDREG
                                   DE $DFFD
                 0070 ARR
                                   DS 02
94A0-
                 0080
                                  LDA #$FF
94A2- A9 FF
                 0090 TRY
94A4- 8D AO 94
                 0100
                                  STA ARR
                                  LDA #$FF
94A7- A9 FF
                 0110
                                  STA ARR+1
94A9- 8D A1 94
                 0120
                                  FHA
                 0125 FIRST
94AC- 48
                                  LOA ARR : FETCH REG DATA
94AD- AD AO 94
                 0130
                                  AND #$OF MASK OFF SECOND NIBBLE
94BO- 29 OF
                 0140
                                  STA DDREG : PLACE DATA ON B BUS
                 0150
94B2- 8D FD DF
                                  JER WR
94B5- 20 E1 94
                 0160
                 0170
                                  LDA ARR : FETCH REG DATA
94B8- AD AO 94
                 0180 SEC
94BB- 29 FO
                                  AND #$FO
                 0190
                                  CLC
94BD- 18
                 0200
                                  ROR A
94BE- 6A
                 0210
                                  ROR A
                 0220
94BF- 6A
9400- 6A
                 0230
                                  ROR A
                                  RUR A
9401- 6A
                 0240
                                  ORA #$10 :ADD REG ADDRESS TO 84&85
9402- 09 10
                 0250
9404- 8D FD DF
                 0260
                                  STA DDREG
9407- 20 E1
            94
                 0270
                                  JER WR
                 0280
                                  LDA ARR+1
                                             FETCH REG DATA
240A- AD A1
            94
                 0290 THRD
940D- 29 OF
                                  AND #$OF
                 0300
940F- 09 20
                 0310
                                  ORA #$20 : ADD REG ADDR
94D1- 8D FD DF
                                  STA DOREG
                                               PLACE ON B BUS
                 0320
94D4- 20 E1
            94
                                  JER WR
                 0330
                 0340
                                  LDA #$30
                 0350 OUT
                                                         : REG ADDR 03
94D7- A9 30
9409- 8D FD DF
                                  STA DOREG
                 0360
94DC- 20 E1 94
                 0370
                                  JER WR
94DF- 68
                                  PLA
                 0375
                                  RTS
94EO- 60
                 0380
                 0390
94E1- A9 05
                 0400 WR
                                  LDA #5
                                  STA CTBUF : ACTIVATE DAG WR LINE
94E3- 8D FC DF
                 0410
94E6- A9 00
                 0420
                                  LDA #00
                                  STA CTBUF : RESET CTRL REG
94E8- 8D FC DF
                 0430
94EB- 60
                 0440
                                  RTS
                 0450
94EC- 48
                 0460 CLDAC
                                  PHA
                                  LDA #$14 : LOWER DAG CLEAR LINE
94ED- A9 14
                 0470
94EF- 8D FC DF
                                  STA CTBUF
                 0480
94F2- A9
         10
                 0490
                                  LDA #$10 : CLEAR CTRL REG
94F4- 8D FC DF
                 0500
                                  STA CTBUF
```

94F7- 68 0505 PLA 94F8- 60 0510 RTS 0520 EN

END OF MAE PASS!

--- LABEL FILE: ---

ARR =94A0 DDREG =DFFD SEC =94B8 WR =94E1 //0000,94F9,94F9 CLDAC =94EC FIRST =94AC THRD =94CA OTBUE =OFFO OUT =94D7 TRY =94A2



## ADDEDNUM FOR DATA 1

To make the DATA 1 Board read both positive and negative input, you need to add the following Basic statements:

1121 LET T = PEEK(A) AND 32

1122 IF T>O THEN PRINT"+";

1123 IF T=O THEN PRINT"-";

You can also do the same to check for overrange:

1124 LET U=PEEK(A) AND 16
1125 IF T>O PRINT"OVERRANGE";

If you want to change the  ${\rm D/A}$  voltage reference, you can do the following:

OUTPUT VOLTAGE	PIN PROGRAMMING
1- 7.5V	Connect pin 2 to pin $3(U20)$ or connect Jumper D to F
2- 5.0V	Connect pin 2 to pin $1(U20)$ or connect Jumper B to D
3- 2.5V	Connect pin 3 to pin $1(U20)$ or connect jumper B to F