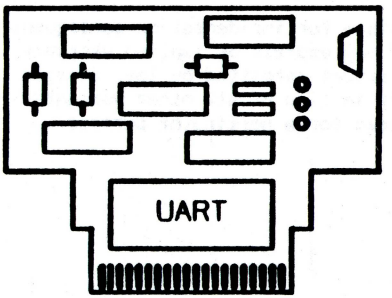
ATRONICS

HART

HIGH SPEED SERIAL UART INTERFACE

FOR THE COMMODORE C128/64

by MARK HATTEN



HART
[HATRONICS Asynchronous Receiver/Transmitter]

LIMITED WARRANTY

HATRONICS is not responsible for incidental or consequential damages resulting from breach of any express or implied warranty, including damage to property and, to the extent permitted by law, damages for personal injury. This warranty is in lieu of all other warranties or merchantability and fitness for a particular purpose..

SPECIAL THANKS TO:

ED BELL
MAT DESMOND
MARV SHELTON

* Parts Placement Notes

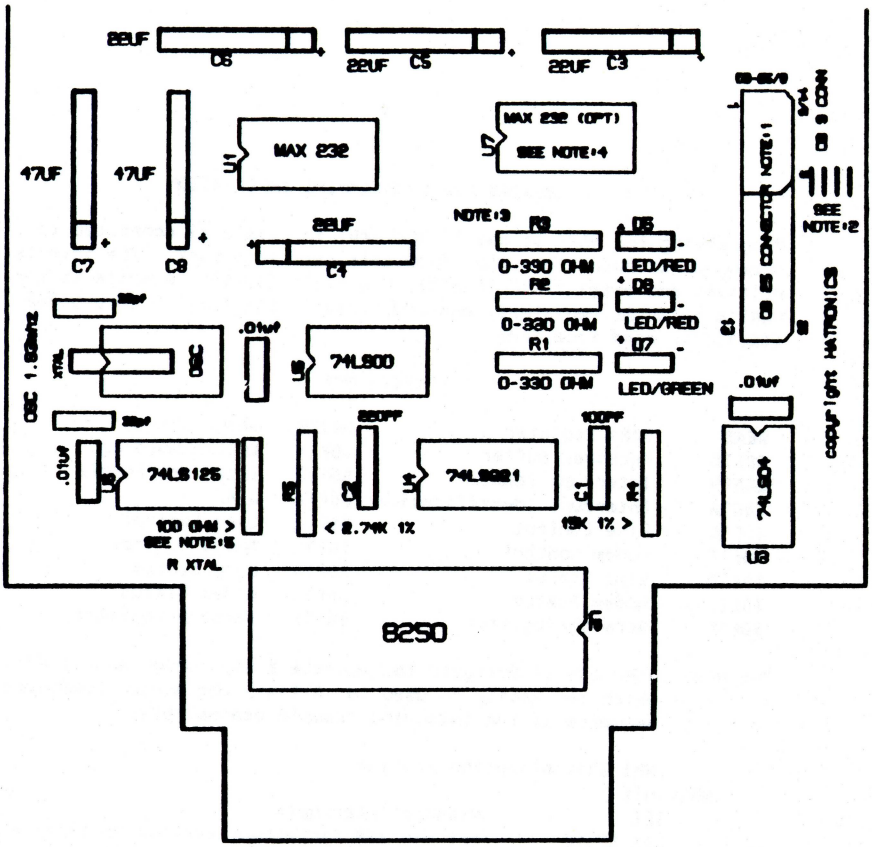
* Note #1 and 2.
The HART pc board is designed to accept a DB-25 connector. To use a DB-25 connector it is necessary to open four jumpers that are on the solder side of the pc board. A flat head screw driver can be used to break open these connection. Care should be taken not to open any other connections. Female connectors should be mounted on the component side while male connectors should be mounted on the solder side of the board.

The use of a DB-9 connector was intended to be a usable option, but was not implemented properly due to the use of a none standard manufacturers spec. The pin outs are defined in the software docs under "Assembly". To utilize a DB-9 a spcial cable would have to be made. The on-board jumpers that were talked about for the DB-25 connector must remain intact.

* Note #3.
Resisters can be used to limit the current to the LEDs but are not mandatory. These positions can be jumped with component lead. The LEDs are brighter without resisters.

* Note #4.
The HART can has the majority of the signals needed for a full RS-232 implementation minus the RI signal. Two MAX 232s are needed to have all the signals active. If only a 3 wire connection is desired then U7 does not have to be installed. With U1 install the TX,RX,RTS and CTS signals are active.

* Note #5.
There are two baud rate clock options designed into the HART pc board. A crystal osc or a crystal can be installed. The plan crystal will need componets R xtal and two 32pf caps. DO NOT install these additional components if a oscillator is used.


22UF C6
22UF C5
22UF C3
47UF
47UF
C7
C9
MAX 232
U1
MAX 232 (OPT)
SEE NOTE:4
U7
22UF
C4
NOTE:3
R3
0-330 OHM
D5
LED/RED
R2
0-330 OHM
D6
LED/RED
R1
0-330 OHM
D7
LED/GREEN
DB-25/F
DB 25 CONNECTOR NOTE:1
P1
P2
DB 9 CONN
SEE NOTE:2
COPYRIGHT HATRONICS
OSC 1.8432MHz
XTAL
OSC
.01uF
74LS00
U6
.01uF
74LS125
U5
100 OHM >
SEE NOTE:5
R XTAL
R5
220PF
C2
74LS221
U4
100PF
C1
19K 1% >
R4
< 8.74K 1%
.01uF
74LS04
U3
8250
U2

HART
(HATRONICS Asynchronous Receiver/Transmitter)

The HART is a deluxe, high-speed RS-232 interface designed specifically for the Commodore C-64, C-128 and C-128D computers. The HART interface is capable of sustaining interrupt driven serial-to-parallel and parallel-to-serial data conversions at spee ds in excess of 19200 baud. The HART is also FULLY PROGRAMMABLE in Commodore BASIC, 6502 and 8502 Assembler and other programming languages.

The center of the HART's design lies in the National Semiconductor NS8250A UART (Universal Asynchronous Receiver Transmitter). This is the same device that is found in the popular IBM PC, XT, AT and compatible computers. The NS8250A UART features:

- Full prioritized interrupt system controls
- Internal diagnostic capabilities
- Line break generation and detection
- TRI-STATE TTL drive capabilities for bidirectional data bus
- Complete status reporting capabilities
- False start bit detection
  Full programmable serial-interface characteristics:
  - 5, 6, 7, or 8 bit characters
  - even, odd, or no parity bit detection and generation
  - 1, 1 1/2, or 2 stop bit generation
  - baud generation
- Modem control functions (CTS,RTS,DSR,DTR,and DCD)
- Independent receiver clock input
- Programmable baud generator
- Independently controlled transmit, receive, and line status
- Full double buffering

DESIGN AND PROGRAMMING INFORMATION

Programming the HART is easy! The HART interface is connected to the Commodore computer thru the computer's cartridge port. The interface utilizes addresses 57112 ($DF18) thru 57118 ($DF1E) to write to the HART's internal registers, and addresses 56 856 ($DE18) thru 56862 ($DE1E) to read from them.

Memory Map

READ	UART Register	WRITE	UART Register
$DE18	Receiver Buffer	$DF18	Xmiter Holding
$DE19	Interrupt Enable	$DF19	Interrupt Enable
$DE1A	Interrupt Identification	$DF1A	N/A
$DE1B	Line Control	$DF1B	Line Control
$DE1C	Modem Control	$DF1C	Modem Control
$DE1D	Line Status	$DF1D	Line Status
$DE1E	Modem Status	$DF1E	Modem Status
$DE1F	Scratch Register	$DF1F	Scratch Register

The HART interface is designed to generate a user programmable NMI interrupt which can easily be used to initiate the normal Commodore NMI interrupt sequence as the following example demonstrates.

```
        ;NMI Initialization Routine
    :NMI-init
        SEI             ;disable interrupts
        LDA $0318       ;get old ISR (interrupt service routine) address
                        ;low-order byte. [ISR = NMI vector]
        STA $0ISRL      ;store old ISR lo-byte in 0ISRL
        LDA $0319       ;get old ISR address hi-order byte
        STA $0ISRH      ;store old ISR hi-byte in 0ISRH
        LDA #>NISR      ;get NEW ISR lo-byte address (NISRL)
        STA $0318       ;store NMI low
        LDA #<NISR      ;get NEW ISR hi-byte address (NISRH)
        STA $0319       ;store NMI high
        CLI
        RTS
```

```
:NISR
     LDA $DE1A      ;read HART Interrupt Ident. Register
     CMP #$06       ;check for receiver line status interrupt
     BEQ $rls-svc   ;service receiver line status interrupt
     CMP #$04       ;check for received data avail. interrupt
     BEQ $rda-svc   ;service received data avail. interrupt
     CMP #$12       ;check for character timeout interrupt
     BEQ $cti-svc   ;service character timeout interrupt
     CMP #$02       ;check for xmit hld reg. empty interrupt
     BEQ $thr-svc   ;service xmit hld reg. empty interrupt
     CMP #$00       ;check for modem status interrupt
     BEQ $mst-svc   ;service modem status interrupt
     JMP $OISRL     ;service normal CBM interrupts
```

The HART can also be easily programmed in CBM 'native' BASIC, simply by applying the same technique to the BASIC PEEK and POKE statements. (sample code may be included elsewhere).

MISCELLANEOUS INFORMATION:

The HART interface has been tested on C-128 computers using 1571, 1581, 1764, 1700 and 1750 commodore peripherals with NO noticeable conflicts or problems. The HART interface is powered directly by the CBM computer and requires no additional power supply.

HART Technical Reference Information

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$DE1D	Line Status	$DF1D	Line Status
$DE1E	Modem Status	$DF1E	Modem Status
$DE1F	Scratch Register	$DF1F	Scratch Register

BACK COVER